IN THE CLAIMS

Please amend the claims as follows:

Claims 1-5 (Canceled).

Claim 6 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

an inductor provided with a first conductor interconnection formed spirally on the semiconductor substrate;

a first shield structure provided with a second conductor interconnection in a ring having a continuous configuration provided along an outer periphery of the spiral pattern of the inductor except for an opening in a portion of the second conductor interconnection, and the second conductor interconnection is electrically connected to ground potential;

a second shield structure disposed at a layer below the first shield structure such that the first shield structure and second shield structure are in different vertical planes, the first shield structure and the second shield structure each having a perimeter that is partially opened;

the first and second shield structures are arranged such that the openings in the perimeters of the first and second shield structures are not superposed in a stacked state; and

a third shield structure disposed at a layer below the second shield structure, a perimeter of the third shield structure including an opening at a position where the perimeter of the first shield structure is open, an opening at a position where the perimeter of the second shield structure is open, and an opening at another position.

Claim 7 (Previously Presented): A semiconductor device according to Claim 6, wherein an interconnection width of the first shield structure is equal to or more than a size of

a spacing of the spiral pattern of the inductor, and is equal to or less than a radius of the spiral pattern of the inductor.

Claim 8 (Previously Presented): A semiconductor device according to Claim 6, wherein a distance between the first shield structure and an outer border of the interconnection of the inductor is equal to a spacing of the spiral pattern of the inductor.

Claim 9 (Previously Presented): A semiconductor device according to Claim 6, further comprising:

a plurality of interconnection layers formed on the semiconductor substrate, each of the plurality of interconnection layers corresponding to one of the first shield structure, second shield structure, and third shield structure, wherein the inductor is formed in any one of these interconnection layers; and

the second conductor interconnection is formed in a different interconnection layer from the interconnection layer in which the inductor is formed.

Claim 10 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

an inductor provided with a first conductor interconnection formed spirally on the semiconductor substrate; and

a first shield structure provided with a second conductor interconnection in a ring having a continuous configuration provided along an inner periphery of the spiral pattern of the inductor except for an opening in a portion of the second conductor interconnection, and the second conductor interconnection is electrically connected to ground potential;

a second shield structure disposed at a layer below the first shield structure such that the first shield structure and second shield structure are in different vertical planes, the first shield structure and the second shield structure each having a perimeter that is partially opened;

the first and second shield structures are arranged such that the openings in the perimeters of the first and second shield structures are not superposed in a stacked state; and

a third shield structure disposed at a layer below the second shield structure, a perimeter of the third shield structure including an opening at a position where the perimeter of the first shield structure is open, an opening at a position where the perimeter of the second shield structure is open, and an opening at another position.

Claim 11 (Previously Presented): A semiconductor device according to Claim 10, wherein an interconnection width of the first shield structure is equal to or less than a size of an interconnection width of the inductor.

Claim 12 (Canceled).

Claim 13 (New). The semiconductor device of claim 1, wherein the second conductor interconnection includes a plurality of notch portions configured to intercept a path of induced current generated by electromagnetic induction from the inductor.

Claim 14 (New). The semiconductor device of claim 10, wherein the second conductor interconnection includes a plurality of notch portions configured to intercept a path of induced current generated by electromagnetic induction from the inductor.

Claim 15 (New). The semiconductor device of claim 1, wherein

a portion of the first shield structure and the inductor are integrally formed together, and

the first shield structure is configured to function as a return path of a signal input to the inductor.

Claim 16 (New). The semiconductor device of claim 10, wherein

a portion of the first shield structure and the inductor are integrally formed together, and

the first shield structure is configured to function as a return path of a signal input to the inductor.